盛新材料科技股份有限公司

Taisic Materials Corp.

TAISIC MATERIALS CORP.

Issue date: 2023/9/1

150mm HPSI substrate	Prime (優選級)	Production (產品級)	Dummy (樣品級)
Type	Semi-Insulating SiC	Semi-Insulating SiC	Semi-Insulating SiC
Material type	SiC-4HSI	SiC-4HSI	SiC-4HSI
Diameter	150 ± 0.25mm	150 ± 0.25mm	150 ± 0.25mm
Thickness	500 ± 25um	500 ± 25um	500 ± 25um
Dopant	un-doped or Vanadium	un-doped or Vanadium	un-doped or Vanadium
Resistivity (Ohm-cm)	≧1e9	≧1e7	≧1e5
Surface orientation	c-plane (0001), ± 0.2°	c-plane (0001), ± 0.25°	c-plane (0001), ± 2°
Si-face	CMP	CMP	CMP
C-face	Polished	Polished	Polished
Bisector of notch deep	1(+0.25,-0)mm	1(+0.25,-0)mm	1(+0.25,-0)mm
Bisector of notch orientation	[1-100] ± 5°	[1-100] ± 5°	[1-100] ± 5°
TTV	≦ 10 um	≦ 10 um	≦ 10 um
LTV(10 X 10mm) (LTV_Avg)	≦ 3 um	≦ 3 um	≦ 4 um
Warp	≦ 35 um	≦ 40um	≦ 50um
Bow (±)	≦ 25 um	≦ 30um	≦ 40um
Crack by high intensity light	None permitted	None permitted	None permitted
Striations by high intensity light	None permitted	None permitted	10 allowed ≦ 10mm each
Scratch by optical surface inspection	≦ 5 scratches and Cumulative length ≦100 mm	≦ 5 scratches and Cumulative length ≦150 mm	≦ 10 scratches and Cumulative length ≦200 mm
Edge exclusion area	3mm	3mm	3mm
Micropipe Density (pcs/cm2)	≦ 0.5cm-2 for 100% of the wafers	≦ 1cm-2 for 100% of the wafers	≦ 10cm-2 for 100% of the wafers
Chipping at the wafer edge	None permitted ≧ 0.5mm width and depth	None permitted ≧ 0.5mm width and depth	Max. 5 pcs ≦ 5mm width and depth
Total usable area* Quantitative by automated optical surface inspection and 2mmx2mm site map	≧ 95% area	≧ 90% area	≧ 50% area
Polytype areas by diffuse lighting	≦ 1%	≦ 5%	≦10%
HEX plates by high intensity light	None permitted	None permitted	≦10%
Contamination (stains/discolored/mottled/cloudy) by high intensity light	None permitted	None permitted	≦10%